HD74AC175

Quad D-Type Flip-Flop

HITACHI

Description

The HD74AC175 is a high-speed quad D flip-flop. The device is useful for general flip-flop requirements where clock and clear inputs are common. The information on the D inputs is stored during the Low-to-High clock transition. Both true and complemented outputs of each flip-flop are provided. A Master Reset input resets all flip-flops, independent of the Clock or D inputs, when Low.

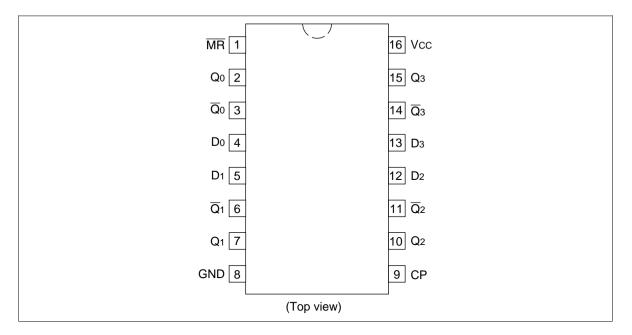
Features

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Asynchronous Common Reset
- True and Complement Output
- Outputs Source/Sink 24 mA

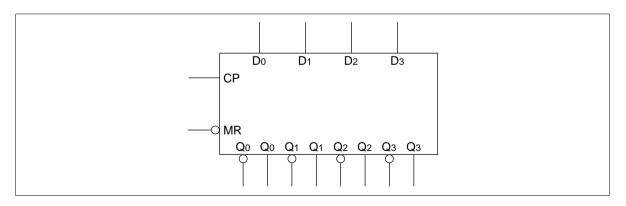


HD74AC175

Pin Arrangement



Logic Symbol



Pin Names

D₀ to D₃ Data Inputs

 $\begin{array}{ll} \hbox{CP} & \hbox{Clock Pulse Input} \\ \hline \hbox{MR} & \hbox{Master Reset Input} \end{array}$

 Q_0 to Q_3 True Outputs

 $\overline{\overline{Q}}_0$ to $\overline{\overline{Q}}_3$ Complement Outputs

Functional Description

The HD74AC175 consists of four edge-triggered D flip-flops with individual D inputs and Q and \overline{Q} outputs. The Clock and Master Reset are common. The four flip-flops will store the state of their individual D inputs on the Low-to-High clock (CP) transition, causing individual Q and \overline{Q} outputs to follow. A Low input on the Master Reset (\overline{MR}) will force all Q outputs Low and \overline{Q} outputs High independent of Clock or Data inputs. The HD74AC175 is useful for general logic applications where a common Master Reset and Clock are acceptable.

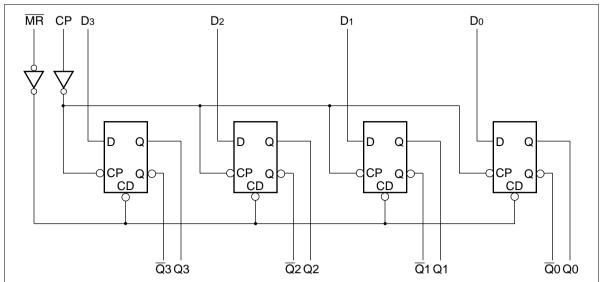
Truth Table

Inputs	Outputs	
@ t _n , MR = H	@ t _{n+1}	
Dn	Qn	Q n
L	L	Н
Н	Н	L

H: High Voltage LevelL: Low Voltage Level

t_n: Bit Time before Clock Pulset_{n+1}: Bit Time after Clock Pulse

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I _{cc}	80	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = Worst case
Maximum quiescent supply current	I _{cc}	8.0	μΑ	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 \text{ V}$, Ta = 25°C

AC Characteristics

			Ta = +25°C C _L = 50 pF		Ta = -40 °C to $+85$ °C C _L = 50 pF			
Item	Symbol	V _{cc} (V)*1	Min	Тур	Max	Min	Max	Unit
Maximum clock	\mathbf{f}_{max}	3.3	149	_	_	139	_	MHz
frequency		5.0	187	_	_	187	_	
Propagation delay	t _{PLH}	3.3	1.0	9.5	12.0	1.0	13.5	ns
CP to Q_{n} or \overline{Q}_{n}		5.0	1.0	7.0	9.0	1.0	9.5	
Propagation delay	t _{PHL}	3.3	1.0	8.5	13.0	1.0	14.5	ns
CP to $Q_{\scriptscriptstyle n}$ or $\overline{Q}_{\scriptscriptstyle n}$		5.0	1.0	6.0	9.5	1.0	10.5	
Propagation delay	t _{PLH}	3.3	1.0	7.5	12.5	1.0	13.5	ns
\overline{MR} to \overline{Q}_n		5.0	1.0	5.5	9.0	1.0	10.0	
Propagation delay	t _{PHL}	3.3	1.0	8.5	11.0	1.0	12.5	ns
$\overline{\text{MR}}$ to Q_n		5.0	1.0	6.0	8.5	1.0	9.5	

Note: 1. Voltage Range 3.3 is 3.3 V \pm 0.3 V Voltage Range 5.0 is 5.0 V \pm 0.5 V

AC Operating Requirements

			Ta = +25°C C _L = 50 pF		Ta = −40°C to +85°C C _L = 50 pF	
Item	Symbol	V _{cc} (V)*1	Тур	Guarante	ed Minimum	Unit
Set-up time, HIGH or LOW	t _{su}	3.3	2.0	4.5	4.5	ns
D _n to CP		5.0	1.0	3.0	3.0	_
Hold time, HIGH or LOW	t _h	3.3	0	1.0	1.0	ns
D _n to CP		5.0	0	1.0	1.0	_
CP pulse width HIGH or LOW	t _w	3.3	2.5	4.5	4.5	ns
		5.0	2.0	3.5	3.5	_
MR pulse width, LOW	t _w	3.3	2.5	4.5	5.0	ns
		5.0	2.0	3.5	3.5	_
Recovery time MR to CP	t _{rec}	3.3	-2.0	0.0	0.0	ns
		5.0	-1.0	0.0	0.0	_

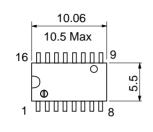
Note: 1. Voltage Range 3.3 is 3.3 V \pm 0.3 V Voltage Range 5.0 is 5.0 V \pm 0.5 V

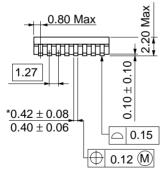
Capacitance

Item	Symbol	Тур	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	45.0	pF	V _{CC} = 5.0 V

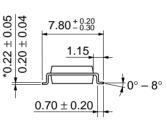
Unit: mm 19.20 20.00 Max 16 7.40 Max 6.30 1.3 1.11 Max 7.62 5.06 Max 2.54 Min 0.51 Min $0.25^{+0.13}_{-0.05}$ 0.48 ± 0.10 2.54 ± 0.25 $0^{\circ} - 15^{\circ}$ Hitachi Code DP-16 **JEDEC** Conforms EIAJ Conforms Weight (reference value) 1.07 g

Unit: mm





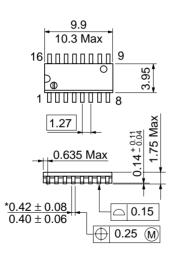


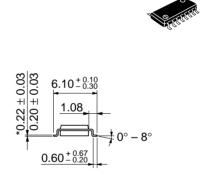


Hitachi Code	FP-16DA
JEDEC	
EIAJ	Conforms
Weight (reference value)	0.24 a

*Dimension including the plating thickness
Base material dimension

Unit: mm

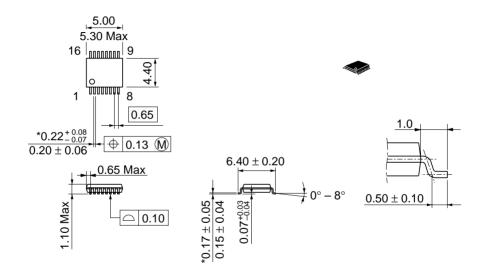




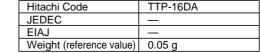
*Dimension including the plating thickness Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

Unit: mm



*Dimension including the plating thickness
Base material dimension



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